REMARKS

Claims 8-11 have been objected to due to informalities. The claims have been amended in accordance with the Examiner's suggestions. In this regard, however, it appears that the proposed insertion of "and" after "parameters" is inappropriate.

Claims 8 and 9 have been rejected under 35 USC 102(e) as anticipated by Solomon (U.S. Pat. No. 6,011,801). The rejection is respectfully traversed.

The present invention discloses a high-level data link controller HDLC, which is based on a time slot oriented controller that can be divided into one or more HDLC channels through configuration of time slot allocation. The HDLC controller is divided into three functional units, namely, bit processing (first stage), time slot/byte processing (second stage) and frame processing (third stage).

The first stage performs time slot allocation and serial/parallel or parallel/serial conversion. To process a time slot, the condition parameters (e.g. time slot length, condition, bit counter, slide register content, etc.) are loaded into the stage at the beginning of the time slot. At the end of a time slot, this stage provides the condition parameters for securing purposes. During the processing of a time slot, the complete data are output or input in a data port. In the second stage, parameters of the next time slot are loaded into the first stage and the parameters of the last time slot are secured. If necessary, this stage also captures data words form the S/P converter or reloads them into the P/S converter. The data are then forwarded to the third stage through separate queues. In the third stage, there is a protocol unit in which the data words are combined into data frames. This unit is responsible for address recognition, block securing and, if applicable, additional protocol functions.

Solomon, on the other hand, discloses data flow between a master and slave module. In this regard, FIFO memories are used., as indicated by the Examiner on page 3 of the Office Action, referring to Figure 7 of Solomon. However, these FIFOs are each located within the master 53 and only illustrate data flow between a master and slave device, as shown in Figure 7 and col. 9, lns. 22-

31. Clearly, these FIFOs are not "processing units" as recited in the claimed invention. Specifically, referring to, for example, to Figure 3 of the instant invention, a high level data link controller HDLC is discloses which includes an HDLC receiver, HDLC transmitter, HDLC processor and buffer. As noted, the controller is essentially divided into three processing units, which processing units are described above. Hence, while Solomon may disclose the transfer of data from one FIFO to another FIFO, those FIFOs do not process the information as required by the claimed invention. For example, the first processing unit reads data out from a current time slot and offering current state parameters of the current time slot, for intermediately storing state parameters of a time slot following the current time slot, and for intermediately storing readout data of the time slot in a first memory unit; the second processing unit with an allocation unit for administering a second memory unit in which the state parameters read out from the first memory unit given a time slot change are stored, for editing the state parameters intermediately stored in the first memory unit, and for allocation of the data of the current time slot intermediately stored in the first memory unit into a third memory unit; and the third processing unit for forming data words from the data deposited in the third memory unit. None of the processes recited in the claims are taught or suggested by Solomon.

Claims 10 and 11 are allowable if rewritten to overcome the objection. The claims having been amended to overcome the objections, now stand in condition for allowance.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no.

449122031100. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

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